--CLK\_50MHz = PIN\_Y2 (50MHz Clock)

--BUZZ = PIN\_AE22 (GPIO 18)

library IEEE;

use IEEE.STD\_LOGIC\_1164.all;

use IEEE.STD\_LOGIC\_ARITH.all;

use IEEE.STD\_LOGIC\_UNSIGNED.all;

entity mid\_C is

port(

CLK\_50MHz : in std\_logic;

BUZZ : out std\_logic);

end mid\_C;

architecture Behavior of mid\_C is

signal counter : std\_logic\_vector(9 downto 0);

signal CLK\_1Hz : std\_logic;

begin

Prescaler: process(CLK\_50MHz)

begin

if CLK\_50MHz'event and CLK\_50MHz = '1' then

if counter < "100000110" then

counter <= counter + 1;

else

CLK\_1Hz <= not CLK\_1Hz;

counter <= (others => '0');

end if;

end if;

end process Prescaler;

BUZZ <= CLK\_1Hz;

end Behavior;

